L Number	Hits	Search Text	DB	Time stamp
55	3	("4575748" | "4578697" | "4789889").PN.	USPAT	2003/08/04 13:14
64	360	29/827,832,840,841,838,839.ccls. and lead$1frame	USPAT; EPO; JPO	2003/08/04 13:56
65	155	(29/827,832,840,841,838,839.ccls. and lead$1frame) and encapsulat$3	USPAT; EPO; JPO	2003/08/04 13:57
95	6	257/666-676.ccls. and lead$1frame and arcuate	USPAT; US-PGPUB	2003/08/04 14:52
96	6	257/666-676.ccls. and lead$1frame and arcuate	USPAT; EPO; JPO	2003/08/04 14:52
97	42	257/666-676.ccls. and lead$1frame and spacing and constant	USPAT; EPO; JPO	2003/08/04 16:08
98	8	("3680206" | "3936930" | "3971610" | "4000054" | "4116517" | "4403272" | "4758459" | "4813129").PN.	USPAT	2003/08/04 16:07
99	1	4453795.pn.	USPAT; EPO; JPO	2003/08/04 16:08
108	45	5313096.URPN.	USPAT	2003/08/04 16:20
129	55	5200362.URPN.	USPAT	2003/08/04 16:37
134	9	("4743956" | "4974053" | "5115298" | "5138430" | "5200364" | "5313102" | "5397916" | "5457340" | "5569956").PN.	USPAT	2003/08/04 18:03
-	2	(leadframe).ti. and (harrison).in.	USPAT; US-PGPUB; EPO; JPO	2003/06/26 17:08
-	9	("4743956" | "4974053" | "5115298" | "5138430" | "5200364" | "5313102" | "5397916" | "5457340" | "5569956").PN.	USPAT	2003/06/26 17:05
-	1387	lead$1frame and encapsulat$3	USPAT; EPO; JPO	2003/06/26 17:09
-	76	(lead$1frame and encapsulat$3) and conductive adj1 pad	USPAT; EPO; JPO	2003/06/26 17:40
-	535	encapsulat$3 and print$3 and lead and conductive adj1 pad	USPAT; EPO; JPO	2003/06/26 17:41

US 5313102 A	19940517	Integrated circuit device having a polyimide moisture barrier coating	257/787	Lim, Thiam B. et al.
US 5457340 A	19951010	Leadframe with power and ground planes	257/666	Templeton, Jr., Thomas H. et
US 6362426 B1	20020326	Radiused leadframe	174/52.2	Harrison, Ronnie M. et al.
US 4743956 A	19880510	Offset bending of curvaceously planar radiating leadframe leads in semiconductor chip packaging	257/674	Olla, Michael A. et al.
US 5138430 A	19920811	High performance versatile thermally enhanced IC chip mounting	257/712	Gow, 3rd, John et al.
US 4974053 A	19901127	Semiconductor device for multiple packaging configurations	257/666	Kinoshita, Mitsuya et al.
US 5594234 A	19970114	Downset exposed die mount pad leadframe and package	257/676	Carter, Jr., Buford H. et al.
US 6165021 A	20001226	Connector for a smart card reader apparatus and card reader comprising same	439/630	Bourne, Frederic
US 5313096 A	19940517	IC chip package having chip attached to and wire bonded within an overlying substrate	257/686	Eide, Floyd K.
US 5158466 A	19921027	Metallically encapsulated elevated interconnection feature	439/67	Schreiber, Christopher M. et
US 5036380 A	19910730	Burn-in pads for tab interconnects	257/668	Chase, Richard A.
US 4774635 A	19880927	Semiconductor package with high density I/O lead connection	361/813	Greenberg, Lawrence A. et al
US 4598337 A	19860701	Electronic circuit board for a timepiece	361/763	Wuthrich, Paul et al.
US 5589402 A	19961231	Process for manufacturing a package for mating with a bare semiconductor die	438/64	Ramsey, Kenneth C. et al.
US 5275975 A	19940104	Method of making a relatively flat semiconductor package having a semiconductor chip encapsulated	438/15	Baudouin, Daniel A. et al.
US 5200364 A	19930406	Packaged integrated circuit with encapsulated electronic devices	29/827	Loh, Wah K.
US 5200362 A	19930406	Method of attaching conductive traces to an encapsulated semiconductor die using a removable tran	29/841	Lin, Paul T. et al.
US 4807018 A	19890221	Method and package for dissipating heat generated by an integrated circuit chip	257/675	Cellai, Marino
US 5939775 A	19990817	Leadframe structure and process for packaging intergrated circuits	257/667	Bucci, Giuseppe D. et al.
US 4453795 A	19840612	Cable-to-cable/component electrical pressure wafer connector assembly	439/361	Moulin, Norbert L.